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Karen Cinq-Mars 8/19/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	August 19, 2003
James S. Mason	:	Examiner:
Serial No.: 10/604,105	:	
Filed: June 26, 2003	:	IBM Corporation Dept. 18G/Bldg, 300-482
Title: ARRANGEMENT, NETWORK AND METHOD FOR REDUCING NON-LINEARITY WITHIN ACTIVE RESISTOR NETWORKS	:	2070 Route 52 Hopewell Junction, NY 12533-6531

CLAIM OF PRIORITY AND CERTIFIED COPY

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Applicant hereby claims foreign priority benefits under 35 USC §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Number	Country	Day/Month/Year
0226800.1	Great Britain	16/11/2002

Applicant encloses a certified copy of the priority document.

Respectfully submitted,
James S. Mason

By Steven Capella
Steven Capella, Attorney
Reg. No. 33,086
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The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

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Dated 19 March 2003

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19NOV02 E764220-1 D00611 1/77
P01/7700 0.00-0226800.1

Patents Act 1977
Rule 16

Request for grant of a patent

The Patent Office
Concept House
Cardiff Road
Newport
South Wales NP10 8QQ

1.	Your reference	GB920020056GB1
2.	Patent application number *(The Patent Office will fill in this part)*	0226800.1 16 NOV 2002
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	INTERNATIONAL BUSINESS MACHINES CORPORATION Armonk New York 10504 United States of America
	Patents ADP number *(if you know it)*	5196370001
	If the applicant is a corporate body, give the country/state of its incorporation	State of New York United States of America
4.	Title of the invention	ARRANGEMENT, NETWORK AND METHOD FOR REDUCING NON-LINEARITY WITHIN ACTIVE RESISTOR NETWORKS
5.	Name of your agent *(if you have one)*	R J Burt
	"Address for Service" in the United Kingdom to which all correspondance should be sent *(including the postcode)*	IBM United Kingdom Limited Intellectual Property Department Hursley Park Winchester Hampshire S021 2JN
	Patents ADP number *(if you know it)*	7903925001

6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country	Priority App No *(if you know it)*	Date of filing *(day/month/year)*
7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date or the earlier application	No of earlier application		Date of filing *(day/month/year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*
a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.)

Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	7
Claim(s)	2
Abstract	1
Drawing(s)	3 + 3

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	2
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application

Signature
R J Burt

14 November 2002
Date

12. Name and daytime telephone number of person to contact in the United Kingdom

P J Stretton
01962 815830

Patents Form 7/77

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7/77

Patents Act 1977
Rule 15

Statement of inventorship and of right to grant of a patent

The Patent Office
Concept House
Cardiff Road
Newport
South Wales NP10 8QQ

1.	Your reference	GB920020056GB1
2.	Patent application number *(if you know it)*	16 NOV 2002 0226800.1
3.	Full name of the or of each applicant	INTERNATIONAL BUSINESS MACHINES CORPORATION
4.	Title of invention	ARRANGEMENT, NETWORK AND METHOD FOR REDUCING NON-LINEARITY WITHIN ACTIVE RESISTOR NETWORKS
5.	State how the applicant(s) derived the right from the inventor(s) to be granted a patent	By employment and by agreement
6.	How many, if any, additional Patents Forms 7/77 are attached to this form?	
7.		I/We believe that the person(s) named over the page (and on any extra copies of this form) is/are the inventor(s) of the invention which the above patent application relates to. Signature R J Burt 14 November 2002 Date
8.	Name and daytime telephone number of person to contact in the United Kingdom	P J Stretton Tel: 01962 815830

Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Patents ADP number *(if known)*
8393142001

Patents ADP number *(if known)*

If there are more than three inventors, please write their names and addresses on the back of another Patents Form 7/77 and attach it to this form

Patents ADP number *(if known)*

REMINDER

Have you signed the form?

ARRANGEMENT, NETWORK AND METHOD FOR REDUCING NON-LINEARITY WITHIN ACTIVE RESISTOR NETWORKS

Field of the Invention

This invention relates to active resistor networks in integrated circuits, and particularly but not exclusively to such active resistor networks in which a transistor such as an Field Effect Transistor (FET) is used to simulate a resistor.

Background of the Invention

In the field of this invention it is known that an FET can be used to model a resistor by operating the device within its ohmic region. There are many circuit applications where this can be desirable, for example in integrated circuit design processes where resistors are not available. In this mode of operation, the FET also provides an advantage in that the value of resistance can also be varied to some extent by controlling the gate bias. This facilitates other applications such as the control of circuit performance (for example, variable gain amplifiers) or to regulate the value of resistance provided by a network.

A well known problem with this arrangement is the so-called resistor non-linearity (resistance change with applied voltage, typically Vds).

When an active resistor is operated away from the bias conditions of the feedback system reference device, in other words when the voltage across the active resistor is different from that applied across the reference, then the resistor value will change. A FET biased in its ohmic region does not exhibit a true linear relationship between current and voltage and so as the voltage across the device alters then so will the resulting resistance.

Various techniques are known which may mitigate the non-linear behaviour of the FET in this operating region, such as selecting an appropriate device geometry and bias condition, but the effect cannot be removed.

In applications where there is a significant change in voltage across the resistor, this non-linearity can cause a substantial impediment to the accuracy of the resistance, and hence the performance of its associated circuitry.

U.S. patent no. 5,793,254 describes a system for controlling an FET to simulate a resistor, which in this case is used to set feedback across an amplifier. However, although this patent suggests that the size of this FET device should be chosen to optimise its performance, and notes that variations in the resistance of the feedback element due to variations in process, temperature, and power supply voltage can affect its performance, it does not address the issue of non-linearity due to changing voltage across the FET device itself. Although the patent describes the addition of a pole-zero circuit which compensates for both the linear and non-linear characteristics of the feedback circuit, it does not directly address one of the most significant non-linear factors, i.e., the change in resistance of the feedback circuit with changing applied voltage across it.

In some applications, the voltage variation can be very significant, for example in termination networks for transmission lines or radio frequency circuits, when the signal may oscillate between zero and its full signal amplitude. The use of FETs for termination in these applications is attractive for integrated circuit applications but the non-linear performance of the device is a strong disincentive.

A need therefore exists for an arrangement, network and method for reducing non-linearity within active resistor networks wherein the abovementioned disadvantages may be alleviated.

Statement of Invention

In accordance with a first aspect of the present invention there is provided an arrangement for reducing non-linearity within an active resistor network, comprising a first active device adapted to provide resistance of a desired resistor, the first active device having a non-linear response; and a second active device coupled to the first active device, the second active device having a non-linear response adapted to compensate substantially for the non-linear response of the first active device.

In accordance with a second aspect of the present invention there is provided an active resistor network comprising the arrangement of the first aspect.

In accordance with a third aspect of the present invention there is provided a method for reducing non-linearity within an active resistor network, comprising providing a first active device adapted to provide resistance of a desired resistor, the first active device having a non-linear response; and providing a second active device coupled to the

first active device, the second active device having a non-linear response adapted to compensate substantially for the non-linear response of the first active device.

The first active device is preferably coupled to receive control signals for regulating the resistance of the arrangement. Preferably the second active device is coupled to receive control signals for regulating the resistance of the arrangement.

Preferably one of the first and second active devices is a p-type device and the other of the first and second active devices is an n-type device.

The first and second active devices are preferably Complementary Metal Oxide Semiconductor devices. Preferably the first and second active devices are provided with minimum dimensions for optimal high frequency performance.

Preferably the first and second active devices are tuned using an optimisation algorithm. Alternatively the first and second active devices are preferably tuned using a manual tuning technique.

In this way an arrangement, network and method for reducing non-linearity within active resistor networks are provided in which non-linear performance with an applied voltage is substantially reduced.

Brief Description of the Drawings

One arrangement, network and method for reducing non-linearity within active resistor networks incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1 shows a block-schematic circuit diagram illustrating a prior art active resistor network utilising a control FET and a reference FET;

FIG. 2 shows a block-schematic circuit diagram illustrating an active resistor network provided with compensation in accordance with a preferred embodiment of the present invention; and

FIG. 3 shows a graph illustrating performance of the arrangement of FIG. 2, with and without compensation.

Description of Preferred Embodiment

Referring to FIG. 1, there is shown a prior art circuit diagram of a basic active resistor control system. A reference resistor element is formed by an N-type FET (NFET) 40, which has a gate electrode driven by the output of a differential amplifier 30.

The differential amplifier 30 also has a non-inverting input coupled via node 35 to a current reference source 10 and an inverting input coupled to a voltage reference source 20. In this way it forms a closed loop controller.

A drain electrode of the NFET 40 is coupled to the node 35, and a source electrode of the NFET 40 is coupled to a common voltage rail 50. The system acts to control the resistance provided by the NFET 40 such that the voltage at its drain electrode (node 35) equals Vref when the drain current is Iref. Consequently, the resistance presented by the NFET 40 is equal to Vref/Iref and the controller output 60 (RBIAS_OUT) can be used to control other networks.

A slave network is formed by an NFET 70, having a gate electrode coupled to the controller output 60, a source electrode coupled to the common voltage rail 50 and a drain electrode coupled to a node 80.

Ignoring matching issues, the resistance presented by the NFET 70 will also be Vref/Iref if the voltage at node 80 is equal to that at node 35. As the voltage at node 80 moves away from that at node 35, an error will be introduced between the resistor values presented by the two networks due to the non-linear behaviour of the NFETs 40 and 70 respectively, when operated within their ohmic region.

As the voltage at node 80 increases beyond that at node 35, the operating point for NFET 70 will move towards the saturation region and the resistance presented by the channel will increase. Similarly, reducing the voltage at node 80 below that at node 35 will tend to reduce the resistance.

Referring now also to FIG. 2, there is shown a circuit diagram of a compensation arrangement according to the invention.

An NFET 220 has a gate electrode coupled to a control input 210, a drain electrode and a source electrode coupled to a common voltage rail 230.

A PFET 240 has a gate electrode coupled to a fixed bias voltage 245 (in this case 0V) relative to the common voltage rail 230, a drain electrode coupled between the drain electrode of the NFET 220 and an output node 250 and a source electrode coupled to the common voltage rail 230.

The inclusion of the second FET, the PFET 240, is designed to counteract and thus substantially compensate for the non-linearity of the NFET 220.

In this case as the voltage at the output 250 increases, resulting in the channel resistance of the NFET 220 increasing, the gate to source voltage of the PFET 240 increases, thereby reducing its channel resistance and providing a compensating effect in the opposite direction.

Since active termination resistors are often connected to a common rail voltage such as the rail 230, this can be used to precisely set the gate and source voltage for the compensating device, in this case the PFET 240. Since the NFET 220 and PFET 240 are complementary devices built in a Complementary Metal Oxide Semiconductor (CMOS) process, their parameters will track to a substantially large degree. Consequently, once the network has been designed, it is possible to control the NFET 220 through a feedback control arrangement (not shown), coupled between the output 250 and the control input 210, in order to regulate the resistance of the overall network.

Alternatively, the feedback control arrangement (not shown) could also be coupled to the fixed bias voltage 245, in order that the PFET 240 also be regulated, in conjunction with the NFET 220, in order to regulate the resistance of the overall network.

The PFET 240 provides the compensation for the non-linearity introduced by the changing drain-source voltage across both FET devices. The size of the NFET 220 and the PFET 240 (width and length of their channels) are chosen to optimise the non-linear performance of the network.

A practical example of the compensation that can be achieved is illustrated by the graph of FIG. 3, which shows how the output resistance (Y-Axis) of a FET can change as the output voltage (X-Axis) moves away from the common rail voltage.

Normally the set point for the closed loop controller (the voltage at node 35 in the example shown in FIG. 1) would nominally be set midway along the operating voltage range of the resistor. In the first case (curve 280), with an uncompensated network, a significant deviation can be observed in

the resistance variation with voltage. Using an appropriately designed network such as that proposed in FIG. 2, this can be significantly improved as shown in the curve 290.

It will be understood that alternative embodiments to that described above are possible. For example, a PFET device could be used as the control element with an NFET device used as the compensation element. However, the basic principle would be the same in all cases, i.e., the adoption of a second device to introduce the non-linearity in the opposite direction to the first device.

The FETs used within the network need to track each other in parametric performance, this solution is ideally suited for integrated circuit applications where device matching is assured.

The two FET sizes need to be selected to achieve both the desired overall resistance value of the network and also to minimise the non-linear effect due to applied voltage across the network. Computer-based optimisation programmes can be used to tune the device sizes for the required performance. Such techniques are well known within circuit design, for example genetic algorithm and simulated annealing are two examples of optimisation techniques that could be used for this problem. Alternatively the network could be manually tuned.

In practice, the device sizes should be minimised for best high frequency performance (there is some trade off between high frequency performance and accuracy, but this is also true for the single FET performance).

Minimising devices sizes, subject to the accuracy constraint, also has the obvious advantage of reducing the area occupied by the network resulting in a more efficient design for IC implementation.

It will also be appreciated that it is also possible to correct for the non-linearity by applying control through the gate voltage of a single device. However, for high frequency applications this would not be a practical solution. The invention described here effectively uses DC control of both gate voltages, a feedback system can be conveniently used to regulate the resistance of the overall network. This approach is convenient for resistors that need to operate at high frequencies.

The same principle could be used for a digitally controlled system. The basic two FET network could be reproduced with binary weights to the

required accuracy. In this case, each weighted network could be controlled by a bit of the binary control bus.

It will also be appreciated that the preferred embodiment described above is particularly suited for active resistor networks which need to operate at high frequencies, for example transmission line terminators, since the additional parasitic capacitance introduced by the compensation device is minimal.

In conclusion, it will be understood that the arrangement, network and method described above provide the following advantages:

- it addresses the non-linear performance with applied voltage (Vds) for FETs operated in the ohmic region.

- it is well suited for high frequency applications as it requires only one extra device and both gates only require a DC bias.

CLAIMS

1. An arrangement for reducing non-linearity within an active resistor network, comprising:

a first active device adapted to provide resistance of a desired resistor, the first active device having a non-linear response; and

a second active device coupled to the first active device, the second active device having a non-linear response adapted to compensate substantially for the non-linear response of the first active device.

2. An active resistor network comprising the arrangement of claim 1.

3. A method for reducing non-linearity within an active resistor network, comprising:

providing a first active device adapted to provide resistance of a desired resistor, the first active device having a non-linear response; and

providing a second active device coupled to the first active device, the second active device having a non-linear response adapted to compensate substantially for the non-linear response of the first active device.

4. The arrangement, network or method of any preceding claim wherein the first active device is coupled to receive control signals for regulating the resistance of the arrangement.

5. The arrangement, network or method of claim 4 wherein the second active device is coupled to receive control signals for regulating the resistance of the arrangement.

6. The arrangement, network or method of any preceding claim wherein one of the first and second active devices is a p-type device and the other of the first and second active devices is an n-type device.

7. The arrangement, network or method of any preceding claim wherein the first and second active devices are Complementary Metal Oxide Semiconductor devices.

8. The arrangement, network or method of any preceding claim wherein the first and second active devices are provided with minimum dimensions for optimal high frequency performance.

9. The arrangement, network or method of any preceding claim wherein the first and second active devices are tuned using an optimisation algorithm.

10. The arrangement, network or method of any one of claims 1 to 8 inclusive wherein the first and second active devices are tuned using a manual tuning technique.

11. An arrangement substantially as hereinbefore described with reference to FIG. 2 and FIG. 3 of the accompanying drawings.

12. A network substantially as hereinbefore described with reference to FIG. 2 and FIG. 3 of the accompanying drawings.

13. A method substantially as hereinbefore described with reference to FIG. 2 and FIG. 3 of the accompanying drawings.

ABSTRACT

ARRANGEMENT, NETWORK AND METHOD FOR REDUCING NON-LINEARITY WITHIN ACTIVE RESISTOR NETWORKS

A compensation arrangement is provided for reducing non-linearity in an active resistor network. A first FET (220) having a non-linear response is provided as an active resistor, and a second FET (240) having a non-linear response is coupled to the first FET (220). The non-linear response of the second FET (240) is adapted in order to compensate for the non-linear response of the first FET (220). The two FETs (220, 240) are complementary, and are selected to achieve the desired overall resistance value of the network. In this way the arrangement substantially reduces non-linear performance with an applied voltage, and is well suited for high frequency applications.

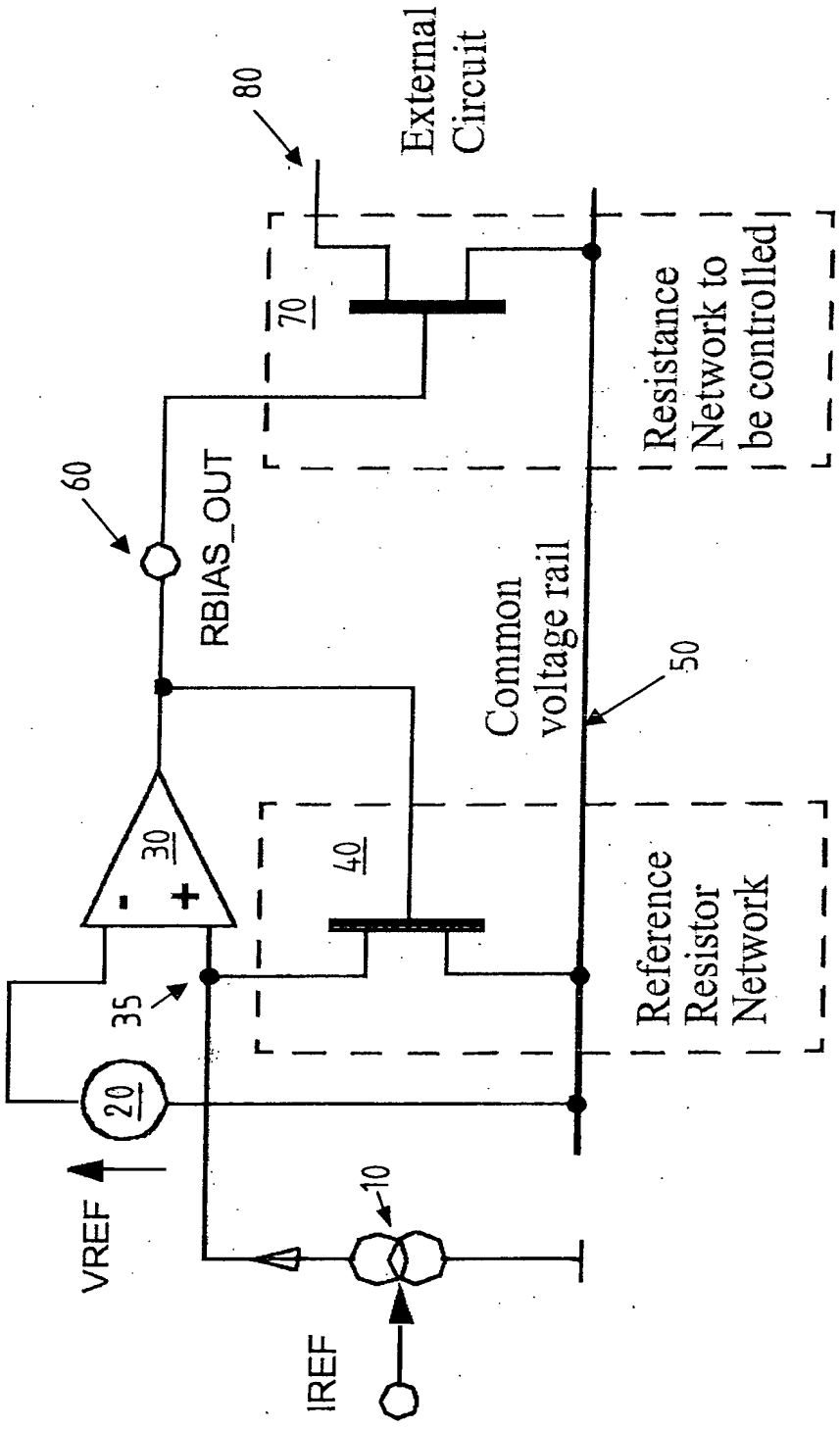

FIG. 1
PRIOR ART

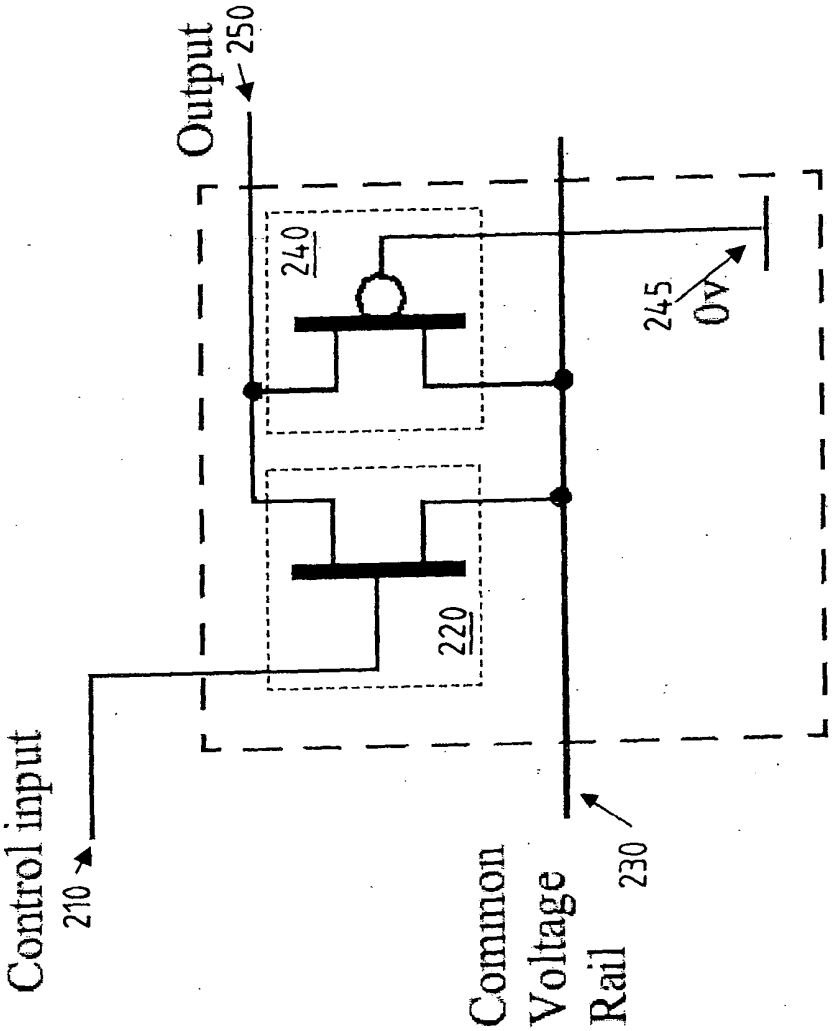
Output
250
240
245
0v
220
Control input
210
Common
Voltage
Rail
230

FIG. 2

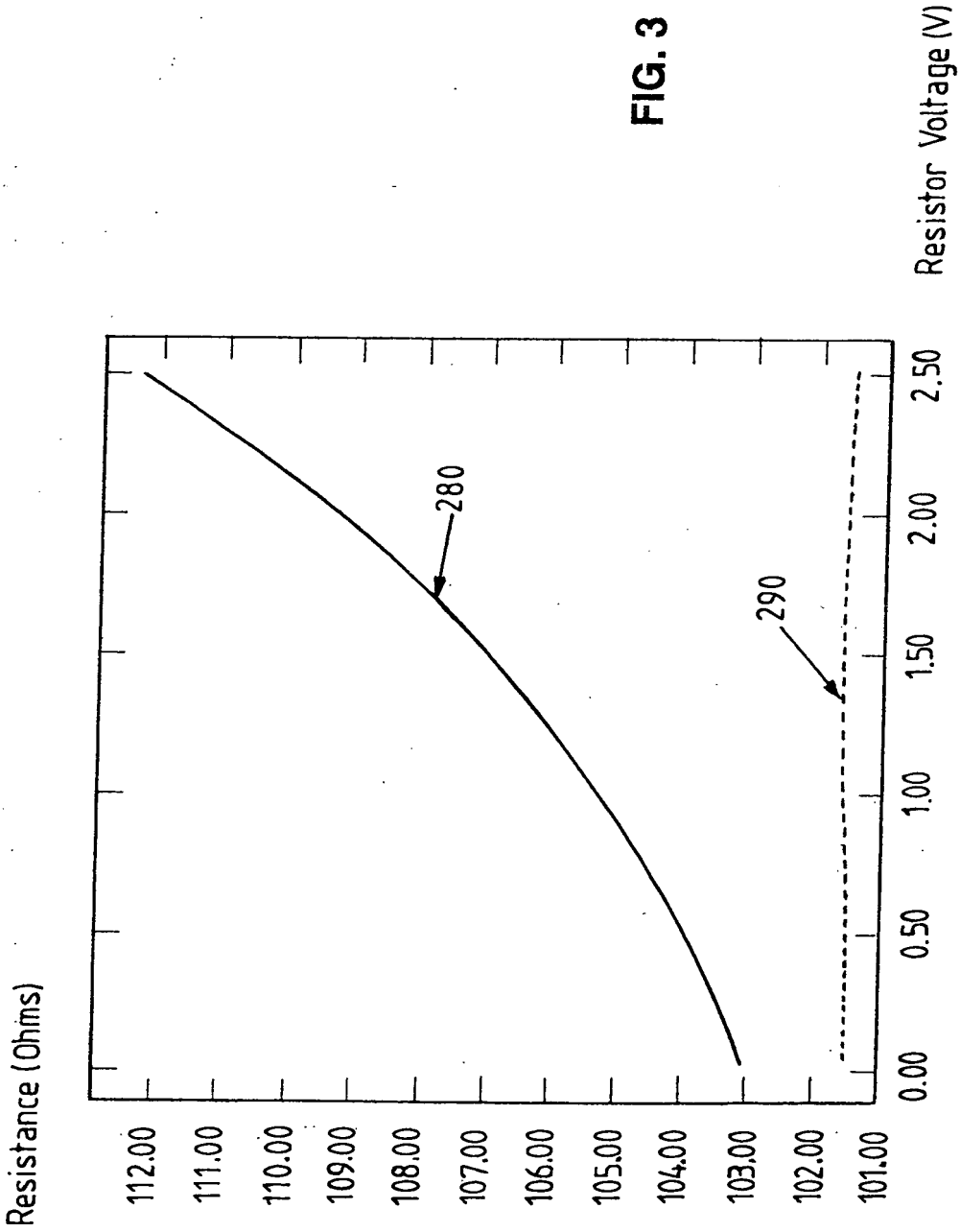
Resistance (Ohms)
112.00
111.00
110.00
109.00
108.00
107.00
106.00
105.00
104.00
103.00
102.00
101.00
0.00
0.50
1.00
1.50
2.00
2.50
Resistor Voltage (V)
280
290

FIG. 3